What is claimed is:

1. A module comprising:

a substrate;

a first microelectronic die mounted on said substrate, said first microelectronic die including a first receiver front end to process a signal received by a first antenna;

a second microelectronic die mounted on said substrate, said second microelectronic die including a second receiver front end to process a signal received by a second antenna;

a third microelectronic die mounted on said substrate, said third microelectronic die including analog baseband circuitry to process baseband output signals of said first and second receiver front ends;

a first interconnect coupled between an output of said first microelectronic die and a first input of said third microelectronic die; and

a second interconnect coupled between an output of said second microelectronic die and a second input of said third microelectronic die.

2. The module of claim 1, wherein:

at least one of said first interconnect and said second interconnect includes a differential transmission line.

3. The module of claim 1, wherein:

at least one of said first interconnect and said second interconnect includes a metallization portion formed on a surface of said substrate.

4. The module of claim 1, wherein:

at least one of said first interconnect and said second interconnect includes a microstrip transmission line formed on said substrate.

5. The module of claim 1, wherein:

said substrate includes a ground plane that forms a part of said first and second interconnects.

6. The module of claim 1, wherein:

said substrate includes a dielectric board material.

7. The module of claim 1, wherein:

said substrate includes alumina.

8. The module of claim 1, wherein:

said substrate includes a semiconductor material.

9. The module of claim 1, comprising:

at least one first terminal for connection to a first external antenna, said at least one first terminal being coupled to said first microelectronic die; and

at least one second terminal for connection to a second external antenna, said at least one second terminal being coupled to said second microelectronic die.

10. The module of claim 1, comprising:

a third interconnect coupled between said first microelectronic die and said second microelectronic die.

11. The module of claim 10, wherein:

said first receiver front end includes a first low noise amplifier (LNA) to amplify a signal from a first antenna and a first mixer to frequency convert an output signal of said first LNA; and

said second receiver front end includes a second LNA to amplify a signal from a second antenna and a second mixer to frequency convert an output signal of said second LNA;

wherein said second microelectronic chip further includes a voltage controlled oscillator to generate local oscillator signals for said first and second mixers, said third interconnect to carry a corresponding local oscillator signal to said first microelectronic die for use by said first mixer.

12. The module of claim 1, comprising:

a fourth microelectronic die mounted on said substrate, said fourth microelectronic die including a third receiver front end to process a signal received by a third antenna; and

a fourth interconnect coupled between an output of said fourth microelectronic die and a third input of said third microelectronic die.

13. A multi-antenna receiver system, comprising:

a first low noise amplifier (LNA) having a differential input to receive a signal from a first antenna;

a second LNA having a single-ended input to receive a signal from a second antenna;

a first mixer to perform a frequency conversion on an amplified output signal of said first LNA;

a second mixer to perform a frequency conversion on an amplified output signal of said second LNA; and

a voltage controlled oscillator (VCO) to provide a local oscillator signal to said first and second mixers.

14. The receiver system of claim 13, wherein:

said first and second LNAs, said first and second mixers, and said VCO are implemented on a common semiconductor chip.

15. The receiver system of claim 13, further comprising:

a first filter to filter a frequency converted output signal of said first mixer, said first filter having an output for connection to a first analog to digital (A/D) converter; and

a second filter to filter a frequency converted output signal of said second mixer, said second filter having an output for connection to a second A/D converter.

16. The receiver system of claim 15, wherein:

said first and second LNAs, said first and second mixers, said VCO, and said first and second filters are implemented on a common semiconductor chip.

17. The receiver system of claim 13, further comprising:

a prescaler to count down an output frequency of said VCO for use in a feedback loop of a corresponding phased locked loop (PLL), wherein said first and second LNAs, said first and second mixers, said VCO, and said prescaler are implemented on a common semiconductor chip.

18. The receiver system of claim 13, further comprising:

a third LNA having a single-ended input to receive a signal from a third antenna; and

a third mixer to perform a frequency conversion on an amplified output signal of said third LNA.

19. A system comprising:

a first patch antenna;

a second patch antenna;

a substrate;

a first microelectronic die mounted on said substrate, said first microelectronic die including a first receiver front end to process a signal received by said first patch antenna;

a second microelectronic die mounted on said substrate, said second microelectronic die including a second receiver front end to process a signal received by said second patch antenna;

a third microelectronic die mounted on said substrate, said third microelectronic die including analog baseband circuitry to process baseband output signals of said first and second receiver front ends;

a first interconnect coupled between an output of said first microelectronic die and a first input of said third microelectronic die; and

a second interconnect coupled between an output of said second microelectronic die and a second input of said third microelectronic die.

20. The system of claim 19, wherein:

said system includes a handheld communicator.

21. The system of claim 19, wherein:

said first and second interconnects include differential transmission lines.

22. The system of claim 19, wherein:

said first and second interconnects include metallization portions formed on a surface of said substrate.

23. The system of claim 19, wherein:

said first and second interconnects are microstrip transmission lines formed on said substrate.

24. The system of claim 19, wherein:

said substrate includes a dielectric board material.

25. The system of claim 19, wherein:

said substrate includes a semiconductor material.

26. The system of claim 19, wherein:

said substrate, said first, second, and third microelectronic dice, and said first and second interconnects are part of a single receiver module.

27. A method comprising:

amplifying a first signal received by a first antenna using a differential low noise amplifier (LNA) to generate an amplified first signal;

amplifying a second signal received by a second antenna using a single ended LNA to generate an amplified second signal; and

processing said amplified first signal and said amplified second signal to generate a single receiver output signal.

28. The method of claim 27, wherein:

processing includes frequency converting said amplified first signal and said amplified second signal.

29. The method of claim 28, wherein:

processing includes filtering said amplified first signal and said amplified second signal after frequency converting.

30. The method of claim 29, wherein:

processing includes converting said amplified first signal and said amplified second signal to a digital format after filtering to generate a digitized first signal and a digitized second signal.

31. The method of claim 30, wherein:

processing includes digitally processing said digitized first signal and said digitized second signal together to generate said single receiver output signal.